

What Is Claimed Is:

- 1 1. An integrated circuit comprising:
 - 2 an output buffer receiving a first value followed by a second value, wherein said first
 - 3 value is not equal to said second value; and
 - 4 a control block changing a strength of said output buffer gradually while said output
 - 5 buffer provides said second value as a buffer output.
- 1 2. The integrated circuit of claim 1, wherein said output buffer comprises a drive
- 2 transistor, and wherein said control block comprises:
 - 3 a capacitor provided at a gate terminal of said drive transistor; and
 - 4 a current source for altering the total charge on said capacitor slowly to change said
 - 5 strength gradually.
- 1 3. The integrated circuit of claim 2, wherein said capacitor comprises a gate
- 2 capacitance of said drive transistor.
- 1 4. The integrated circuit of claim 2, wherein said output buffer comprises a plurality
- 2 of inverters, wherein one of said plurality of inverters comprises said drive transistor.
- 1 5. The integrated circuit of claim 4, wherein said drive transistor is contained in a last
- 2 one of said plurality of inverters.
- 1 6. The integrated circuit of claim 2, wherein said drive transistor comprises a PMOS

2 transistor, wherein said current source discharges said capacitor to control said drive strength
3 when said second value is greater than said first value.

1 7. The integrated circuit of claim 6, wherein said control block comprises:
2 a voltage adjusting block which determines a total strength to be applied to said drive
3 transistor when said second value is greater than said first value, and provides a PCTRL
4 signal representing said total strength; and

5 a slew controller block coupled to said drive transistor, said slew controller block
6 containing said current source, wherein said current source receives said PCTRL to determine
7 the amount of current to supply to discharge said capacitor.

1 8. The integrated circuit of claim 7, wherein said control block comprises:
2 a delay module delaying a clock signal to generate a delayed clock signal, wherein
3 said clock signal is used to control the timing of reception of said first value and said second
4 value; and

5 a comparator comparing said buffer output with a threshold voltage to determine
6 whether said buffer output is rising at a desired rate, said comparator providing a comparison
7 result,

8 wherein said voltage adjusting block adjusts said total strength according to said
9 comparison result.

1 9. The integrated circuit of claim 8, wherein said voltage adjusting block adjusts said
2 total strength in multiple increments until said total strength equals a desired strength,

3 wherein said desired strength is determined by said desired rate.

1 10. The integrated circuit of claim 7, wherein said current source comprises:

2 a first transmission gate which conducts in one logical state of a clock signal and does
3 not conduct on the other logical state of said clock signal, said first transmission gate being
4 connected between a first node and a second node, said second node being coupled to a
5 supply voltage;

6 a second transmission gate being connected between said first node and a third node,
7 said second transmission gate conducting in said other logical state of said clock signal and
8 not conducting in said one logical state of said clock signal, said third node being coupled
9 to receive said PCTRL; and

10 a second capacitor coupled between said first node and said voltage supply, wherein
11 a desired amount of current to discharge said capacitor is generated at said third node.

1 11. The integrated circuit of claim 10, wherein the capacitance of said second
2 capacitor equals the capacitance of said capacitor.

1 12. The integrated circuit of claim 11, wherein said current source further comprises
2 a drop transistor connected between said supply voltage and said second node, said drop
3 transistor providing a voltage drop to apply a voltage of said supply voltage less said voltage
4 drop at said second node so as to switch off said drive transistor.

1 13. The integrated circuit of claim 12, further comprising:

2 a second drop transistor provided between said supply voltage and a gate terminal of
3 said PMOS transistor, wherein said second drop transistor also provides said voltage drop to
4 apply a voltage of said supply voltage less said voltage drop at said gate terminal of said
5 PMOS transistor.

1 14. The integrated circuit of claim 13, further comprising a clamping circuit to clamp
2 the voltage at the gate terminal of said PMOS transistor to said PCTRL.

1 15. The integrated circuit of claim 2, wherein said drive transistor comprises a NMOS
2 transistor, wherein said current source charges said capacitor to control said drive strength
3 when said second value is less than said first value.

1 16. The integrated circuit of claim 6, wherein said control block comprises:
2 a voltage adjusting block which determines a total strength to be applied to said drive
3 transistor when said second value is less than said first value, and provides a NCTRL signal
4 representing said total strength; and

5 a slew controller block coupled to said drive transistor, said slew controller block
6 containing said current source, wherein said current source receives said NCTRL to
7 determine the amount of current to supply to discharge said capacitor.

1 17. The integrated circuit of claim 16, wherein said control block comprises:
2 a delay module delaying a clock signal to generate a delayed clock signal, wherein
3 said clock signal is used to control the timing of reception of said first value and said second

4 value; and

5 a comparator comparing said buffer output with a threshold voltage to determine

6 whether said buffer output is falling at a desired rate, said comparator providing a

7 comparison result,

8 wherein said voltage adjusting block adjusts said total strength according to said

9 comparison result.

1 18. The integrated circuit of claim 13, further comprising a clamping circuit to clamp

2 the voltage at the gate terminal of said NMOS transistor to said NCTRL.

1 19. The integrated circuit of claim 1, wherein said strength is changed such that an

2 output signal of said output buffer changes from a first voltage level representing said first

3 value to a second voltage level representing said second value in a duration which is

4 substantially more than 15% of a clock cycle duration using which said first value and said

5 second value are received.

1 20. The integrated circuit of claim 1, wherein said duration equals at least 40% of said

2 clock cycle duration.

1 21. A device comprising:

2 an output buffer receiving a first value followed by a second value, wherein said first

3 value is not equal to said second value; and

4 a control block changing a strength of said output buffer gradually while said output

5 buffer provides said second value as a buffer output.

1 22. The device of claim 21, wherein said output buffer comprises a drive transistor,
2 and wherein said control block comprises:

3 a capacitor provided at a gate terminal of said drive transistor; and
4 a current source for altering the total charge on said capacitor slowly to change said
5 strength gradually.

1 23. The device of claim 22, wherein said capacitor comprises a gate capacitance of
2 said drive transistor.

1 24. The device of claim 22, wherein said output buffer comprises a plurality of
2 inverters, wherein one of said plurality of inverters comprises said drive transistor.

1 25. The device of claim 24, wherein said drive transistor is contained in a last one of
2 said plurality of inverters.

1 26. The device of claim 22, wherein said drive transistor comprises a PMOS
2 transistor, wherein said current source discharges said capacitor to control said drive strength
3 when said second value is greater than said first value.

1 27. The device of claim 26, wherein said control block comprises:
2 a voltage adjusting block which determines a total strength to be applied to said drive

3 transistor when said second value is greater than said first value, and provides a PCTRL
4 signal representing said total strength; and

5 a slew controller block coupled to said drive transistor, said slew controller block
6 containing said current source, wherein said current source receives said PCTRL to determine
7 the amount of current to supply to discharge said capacitor.

1 28. The device of claim 27, wherein said control block comprises:

2 a delay module delaying a clock signal to generate a delayed clock signal, wherein
3 said clock signal is used to control the timing of reception of said first value and said second
4 value; and

5 a comparator comparing said buffer output with a threshold voltage to determine
6 whether said buffer output is rising at a desired rate, said comparator providing a comparison
7 result,

8 wherein said voltage adjusting block adjusts said total strength according to said
9 comparison result.

1 29. The device of claim 28, wherein said voltage adjusting block adjusts said total
2 strength in multiple increments until said total strength equals a desired strength, wherein
3 said desired strength is determined by said desired rate.

1 30. The device of claim 27, wherein said current source comprises:

2 a first transmission gate which conducts in one logical state of a clock signal and does
3 not conduct on the other logical state of said clock signal, said first transmission gate being

4 connected between a first node and a second node, said second node being coupled to a
5 supply voltage;

6 a second transmission gate being connected between said first node and a third node,
7 said second transmission gate conducting in said other logical state of said clock signal and
8 not conducting in said one logical state of said clock signal, said third node being coupled
9 to receive said PCTRL; and

10 a second capacitor coupled between said first node and said voltage supply, wherein
11 a desired amount of current to discharge said capacitor is generated at said third node.

1 31. The device of claim 30, wherein the capacitance of said second capacitor equals
2 the capacitance of said capacitor.

1 32. The device of claim 31, wherein said current source further comprises a drop
2 transistor connected between said supply voltage and said second node, said drop transistor
3 providing a voltage drop to apply a voltage of said supply voltage less said voltage drop at
4 said second node.

1 33. The device of claim 32, further comprising:
2 a second drop transistor provided between said supply voltage and a gate terminal of
3 said PMOS transistor, wherein said second drop transistor also provides said voltage drop to
4 apply a voltage of said supply voltage less said voltage drop at said gate terminal of said
5 PMOS transistor.

1 34. The device of claim 33, further comprising a clamping circuit to clamp the
2 voltage at the gate terminal of said PMOS transistor to said PCTRL.

1 35. The device of claim 22, wherein said drive transistor comprises a NMOS
2 transistor, wherein said current source charges said capacitor to control said drive strength
3 when said second value is less than said first value.

1 36. The device of claim 26, wherein said control block comprises:
2 a voltage adjusting block which determines a total strength to be applied to said drive
3 transistor when said second value is less than said first value, and provides a NCTRL signal
4 representing said total strength; and
5 a slew controller block coupled to said drive transistor, said slew controller block
6 containing said current source, wherein said current source receives said NCTRL to
7 determine the amount of current to supply to discharge said capacitor.

1 37. The device of claim 36, wherein said control block comprises:
2 a delay module delaying a clock signal to generate a delayed clock signal, wherein
3 said clock signal is used to control the timing of reception of said first value and said second
4 value; and
5 a comparator comparing said buffer output with a threshold voltage to determine
6 whether said buffer output is falling at a desired rate, said comparator providing a
7 comparison result,
8 wherein said voltage adjusting block adjusts said total strength according to said

9 comparison result.

1 38. The device of claim 33, further comprising a clamping circuit to clamp the
2 voltage at the gate terminal of said NMOS transistor to said NCTRL.

1 39. The device of claim 21, wherein said strength is changed such that an output
2 signal of said output buffer changes from a first voltage level representing said first value to
3 a second voltage level representing said second value in a duration which is substantially
4 more than 15% of a clock cycle duration using which said first value and said second value
5 are received.

1 40. The device of claim 21, wherein said duration equals at least 40% of said clock
2 cycle duration.

1 41. The device of claim 21, wherein said device further comprises a load receiving
2 said buffer output.

1 42. The device of claim 41, wherein said load comprises a transmission line.

1 43. The device of claim 21, wherein said device comprises a wireless base station,
2 said device further comprising:
3 an antenna receiving an external signal; and
4 an analog processor processing said external signal to generate said first value and

5 said second value.

1 44. An apparatus comprising:

2 an output buffer receiving a transition from a first value to a second value, wherein
3 said first value is not equal to said second value, said buffer providing said first value
4 followed by said second value on a buffer output; and

5 means for changing a strength of said output buffer gradually while providing said
6 second value on said buffer output.

1 45. The apparatus of claim 44, wherein said output buffer comprises an inverter
2 containing a transistor, wherein said means for changing alters slowly an amount of charge
3 on a capacitor provided at a gate terminal of said transistor.

1 46. The apparatus of claim 45, wherein said capacitor comprises a gate capacitance
2 of said gate terminal.

1 47. The apparatus of claim 45, wherein said means for changing comprises a current
2 source to perform said altering.

1 48. A method of processing a transition from a first value to a second value, wherein
2 said first value is not equal to said second value, said method comprising:
3 receiving said first value followed by said second value on a buffer input of an output
4 buffer;

5 providing said first value on a buffer output of said output buffer; and
6 changing a strength of said output buffer gradually while providing said second value
7 on said buffer output.

1 49. The method of claim 48, wherein said output buffer comprises an inverter
2 containing a transistor, said changing comprises altering slowly an amount of charge on a
3 capacitor provided at a gate terminal of said transistor.

1 50. The method of claim 49, wherein said capacitor comprises a gate capacitance of
2 said gate terminal.

1 51. The method of claim 49, wherein said changing is performed using a current
2 source.

1 52. The method of claim 51, wherein said strength is changed such that an output
2 signal of said output buffer changes from a first voltage level representing said first value to
3 a second voltage level representing said second value in a duration which is substantially
4 more than 15% of a clock cycle duration using which said first value and said second value
5 are received.

1 53. The method of claim 52, wherein said duration equals at least 40% of said clock
2 cycle duration.